AMENDMENTS TO THE CLAIMS

Claim 1. (cancel)

Claim 2. (currently amended): A memory device comprising:

an apparatus for reading data from a programmable conductor random access memory cell, said apparatus comprising:

an access circuit for coupling said memory cell between an addressed and activated word line and an addressed and activated bit line during a read operation;

a sense amplifier coupled to said addressed and activated bit line for sensing a logical state of said memory cell; and

preventing circuitry for preventing said memory cell from being refreshed in response to said read operation;

~~The memory device of claim 1,~~ wherein said access circuit is a transistor circuit and said preventing circuitry causes said activated word line to be deactivated after a logical state of said memory cell is transferred to said activated bit line and before said sense amplifier senses a logical state of said memory cell.

Claim 3. (original): The memory device of claim 2, wherein said preventing circuitry comprises a transistor which causes said activated word line to be deactivated.

Claim 4. (original): The memory device of claim 3, wherein said transistor is serially connected between said word line and a driver for said word line and is turned on during said read operation and turned off to deactivate said row line.

Claim 5. (original): The memory device of claim 3, wherein said transistor is connected between said word line and ground and is turned off during said read operation and is turned on to deactivate said word line.

Claim 6. (currently amended): A memory device comprising:

an apparatus for reading data from a programmable conductor random access memory cell, said apparatus comprising:

an access circuit for coupling said memory cell between an addressed and activated word line and an addressed and activated bit line during a read operation;

a sense amplifier coupled to said addressed and activated bit line for sensing a logical state of said memory cell; and

preventing circuitry for preventing said memory cell from being refreshed in response to said read operation;

~~The memory device of claim 1,~~ wherein said preventing circuitry comprises a transistor serially connected between an activated bit line and a sense amplifier associated with the activate bit line, said serially connected transistor being

turned on during a read operation and turned off before said memory cell can be refreshed.

Claim 7. (currently amended): A memory device comprising:

an apparatus for reading data from a programmable conductor random access memory cell, said apparatus comprising:

an access circuit for coupling said memory cell between an addressed and activated word line and an addressed and activated bit line during a read operation;

a sense amplifier coupled to said addressed and activated bit line for sensing a logical state of said memory cell; and

preventing circuitry for preventing said memory cell from being refreshed in response to said read operation;

~~The memory device of claim 1,~~ wherein said preventing circuitry causes said activated word line to be deactivated a predetermined amount of time after said memory cell begins to transfer a logical state to said activated bit line.

Claim 8. (original): The memory device of claim 7, wherein said sense amplifier further comprises a first sense amplifier portion and a second sense amplifier portion.

Claim 9. (original): The memory device of claim 8, wherein said predetermined amount of time is after said first sense amplifier portion is activated and before said second sense amplifier portion is activated.

Claim 10. (original): The memory device of claim 8, wherein said first sense amplifier portion is a N-sense amplifier, and said second sense amplifier portion is a P-sense amplifier.

Claim 11. (currently amended): The memory device of claim 2, [[1]] further comprising:

a pre-charge circuit for pre-charging the addressed and activated bit line and an another bit line, wherein said addressed and accessed bit line and said other bit line are coupled to the sense amplifier.

Claim 12. (original): The memory device of claim 11, wherein said pre-charge circuit pre-charges the addressed and activated bit line and the another bit line prior to the sense amplifier sensing said addressed and activated bit line.

Claim 13. (cancel):

A system comprising,

a processor; and

a memory, said memory further comprising,

an apparatus for reading data from a programmable conductor random access memory cell, said apparatus comprising:

an access circuit for coupling said memory cell between an addressed and activated word line and an addressed and activated bit line during a read operation;

a sense amplifier coupled to said addressed and activated bit line for sensing a logical state of said memory cell; and

preventing circuitry for preventing said memory cell from being refreshed in response to said read operation.

Claim 14. (currently amended): A system comprising,

a processor; and

a memory, said memory further comprising,

an apparatus for reading data from a programmable conductor random access memory cell, said apparatus comprising:

an access circuit for coupling said memory cell between an addressed and activated word line and an addressed and activated bit line during a read operation;

a sense amplifier coupled to said addressed and activated bit line for sensing a logical state of said memory cell; and

preventing circuitry for preventing said memory cell from being refreshed in response to said read operation;

~~The system of claim 13,~~ wherein said access circuit is a transistor circuit and said preventing circuitry causes said activated word line to be deactivated after a logical state of said memory cell is transferred to said activated bit line and before said sense amplifier senses a logical state of said memory cell.

Claim 15. (original): The system of claim 14, wherein said preventing circuitry comprises a transistor which causes said activated word line to be deactivated.

Claim 16. (original): The system of claim 15, wherein said transistor is serially connected between said word line and a driver for said word line and is turned on during said read operation and turned off to deactivate said row line.

Claim 17. (original): The system of claim 15, wherein said transistor is connected between said word line and ground and is turned off during said read operation and is turned on to deactivate said word line.

Claim 18. (currently amended): A system comprising,

a processor; and

a memory, said memory further comprising,

an apparatus for reading data from a programmable conductor random access memory cell, said apparatus comprising:

an access circuit for coupling said memory cell between an addressed and activated word line and an addressed and activated bit line during a read operation;

a sense amplifier coupled to said addressed and activated bit line for sensing a logical state of said memory cell; and

preventing circuitry for preventing said memory cell from being refreshed in response to said read operation;

~~The system of claim 13,~~ wherein said preventing circuitry comprises a transistor serially connected between an activated bit line and a sense amplifier associated with the activate bit line, said serially connected transistor being turned on during a read operation and turned off before said memory cell can be refreshed.

Claim 19. (currently amended): A system comprising,

a processor; and

a memory, said memory further comprising,

an apparatus for reading data from a programmable conductor random access memory cell, said apparatus comprising:

an access circuit for coupling said memory cell between an addressed and activated word line and an addressed and activated bit line during a read operation;

a sense amplifier coupled to said addressed and activated bit line for sensing a logical state of said memory cell; and

preventing circuitry for preventing said memory cell from being refreshed in response to said read operation;

~~The system of claim 13,~~ wherein said preventing circuitry causes said activated word line to be deactivated a predetermined amount of time after said memory cell begins to transfer a logical state to said activated bit line.

Claim 20. (original): The system of claim 19, wherein said sense amplifier further comprises a first sense amplifier portion and a second sense amplifier portion.

Claim 21. (original): The system of claim 20, wherein said predetermined amount of time is after said first sense amplifier portion is activated and before said second sense amplifier portion is activated.

Claim 22. (original): The system of claim 20, wherein said first sense amplifier portion is a N-sense amplifier and said second sense amplifier portion is a P-sense amplifier.

Claim 23. (currently amended): The system of claim 14, [[13]] further comprising:

a pre-charge circuit for pre-charging the addressed and activated bit line and an another bit line, wherein said addressed and accessed bit line and said other bit line are coupled to the sense amplifier.

Claim 24. (original): The system of claim 23, wherein said pre-charge circuit pre-charges the addressed and activated bit line and the another bit line prior to the sense amplifier sensing said addressed and activated bit line.

Claims 25-38 (cancel)